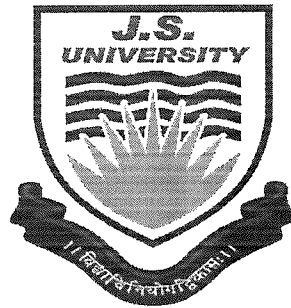


# **J.S. University, Shikohabad**

Established by UP Govt. Act No. 07 of 2015

Recognized by U.G.C. under section 2 (f) of Act-1956



## **Value Added Course**

[VAC-164]

**Circuit Design and Verification using eSim**

**Faculty of Engineering**

**Department of Electrical and Electronics Engineering**



J.S. University, Shikohabad  
Faculty of Engineering

Value Added Course

AY: 2022-23

## VAC-164-Circuit Design and Verification using eSim

### Learning Objective:

Learn module making of Analog electronics components and their functional verification.


**Duration:** 30 Hours. (Theory and Practical)

### Course Outcomes: -

Maximum Exposure has to be given on Practical Oriented

After completion of the course the student shall be able to:-

1. Build modules of components including sequencer, Driver, Monitor etc.
2. Able to configure and design Current Mirrors, Single Stage Amplifier
3. Learn functional verification of Current Mirrors, Single Stage Amplifier
4. Learn self-checking automation on components
5. Design the functional verification of Current Mirrors, Single Stage Amplifier and components

	<b>J.S. University, Shikohabad</b> <b>Faculty of Engineering</b>	<b>Value Added Course</b>
		AY: 2022-23

### Syllabus Outline

**1. Module-1 Advanced Circuit analysis Techniques and Tools**

Real SC circuit analysis, Kirchhoff's law, Basic Circuits, Voltage dividers

**2. Module-2 Basics of eSim**

Installation of eSim, Basic toolbox, software working

**3. Module-3 Building components in eSIM**

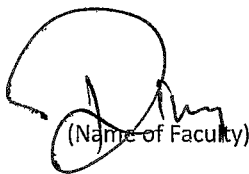
.Selecting working layer, Placing a track between two nodes, Adding Board outline, Adding a ground plane for the board.

**4. Module-4 Creating a Device model**

Introduction to Device Models, Creating a Germanium Diode 1N34A model using the Model Editor feature, Adding parameters of Germanium 1N34A, Obtaining Diode operation Characteristics.

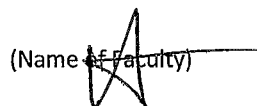
**5. Module-5 Editing Sub-circuit**

Introduction to Edit sub-circuit feature, Editing an existing Half Adder sub-circuit, Adding an Inverter gate to the output of AND gate, adding Port

  
 (Name of Faculty)

Course Coordinator

Er. Divyanshu  
Gupta

  
 (Name of Faculty)

Dean Academics

Dr. Akhilesh

  
 (Name of Faculty)

Director/Principle/Dean of  
Faculty/Department

Dr. Sheikh  
Sudeesh